IN THE DRAWINGS:

1. Attached hereto is Replacement Sheet for FIG. 4 that is labeled "Prior Art" and "Replacement Sheet" in response to the objection made to FIG. 4 as filed.

REMARKS

The Office Action mailed August 23, 2005 objected to FIG. 3, FIG. 4, and FIG. 10 and to the specification at various locations. Applicants herewith submit a Replacement Sheet for FIG. 4, amend the specification to overcome objections to FIG. 3, FIG. 10, and amend the specification to overcome the objects to the specification.

The Office Action objected to claims 8 and 23 because of informalities. Each of claims 8 and 23 are amended herein to address these objections.

The Office Action rejected claims 1, 3-5, 7, 11, 16, 18-20, 22, 26, and 29 under 35 U.S.C. 102(b) as being anticipated by Pukkila (US 20010017904 A1). The Office Action rejected claims 1-7, 9-11, 13-22, 24-26, and 28-31 under 35 U.S.C. 102(e) as being anticipated by Parolari (US 20040081248 A1). The Office Action rejected claims 8, 12, 23, and 27 under 35 U.S.C. 103(a) as being unpatentable over Parolari as applied to claim 1 and further in view of Ramesh (US 6909758 B2). Applicants respectfully traverse the rejections made under 35 U.S.C. 102(b), 102(e), and 103(a).

The Office Action further rejected claims 1, 12, 16, 27, and 31 over co-pending application 10/731,803 under a provisional obvious-type double patenting rejection. With respect to these double-patenting rejections, Applicants will submit a Terminal Disclaimer at such time as is required to overcome the double-patenting rejection.

Claims 1 is not anticipated under 35 U.S.C. 102(b) by Pukkila

Anticipation is established only if (1) all the elements of an invention, as stated in a patent claim, (2) are identically set forth, (3) in a single prior art reference. See, e.g., Gechter v. Davidson, 116 F.3d 1454, 1457, re USPQ2d 1030, 1032 (Fed. Cir. 1997)("Under 35 U.S.C. § 102, every limitation of a claim must identically appear in a single prior art reference for it to anticipate the

claim.") Applicants respectfully assert that Pukkila does not identically disclose all elements of claim 1.

Independent claim 1 is directed to a "method for performing Incremental Redundancy (IR) operations in a wireless receiver." This method includes:

receiving an analog signal corresponding to a data block;

sampling the analog signal to produce samples;

equalizing the samples to produce soft decision bits of the data block;

configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers;

initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver; and

accessing, by the IR processing module, the plurality of IR processing module registers; and

performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block.

Applicant concedes that Pukkila fairly discloses the elements of receiving, sampling, and equalizing of claim 1. Applicants deny that Pukkila discloses, suggests, or teaches the elements of configuring, initiating, accessing, or performing of claim 1.

The Office Action equates block 205' of FIG. 2 and blocks 305-318 of FIG. 3 of Pukkila with "configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers." As Pukkila describes at paragraph 25, last sentence, block 205' is a "turbo equalizer." Block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and reinterleaving operations. Block 205'. Block 205' of FIG. 2 of Pukkila and the associated

operations of FIG. 3 cannot be equated the operations of claim 1 performed by a system processor. Blocks 305-318 do not disclose, suggest, or teach "configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers." Because Pukkila does not identically set forth this element of claim 1, Pukkila does not anticipate claim 1.

The Office Action equates block 205' of FIG. 2 and blocks 305-318 of FIG. 3 of Pukkila with "initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver." As Pukkila describes at paragraph 25, last sentence, block 205' is a "turbo equalizer." Block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and reinterleaving operations. Block 205' of FIG. 2 of Pukkila cannot be equated to a system processor. Further, blocks 305-318 do not disclose, suggest, or teach "initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver." Because Pukkila does not identically set forth this element of claim 1, Pukkila does not anticipate claim 1.

The Office Action equates block 205' of FIG. 2 and blocks 305-318 of FIG. 3 of Pukkila with "accessing, by the IR processing module, the plurality of IR processing module registers." As Pukkila describes at paragraph 25, last sentence, block 205' is a "turbo equalizer." Block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and reinterleaving operations. Block 205' of FIG. 2 of Pukkila cannot be equated with an IR processing module. Further, blocks 305-318 do not disclose, suggest, or teach "accessing, by the IR processing module, the plurality of IR processing module registers." Because Pukkila does not identically set forth this element of claim 1, Pukkila does not anticipate claim 1.

The Office Action equates block 205' of FIG. 2 and blocks 305-318 of FIG. 3 of Pukkila with "performing, by the IR processing module, IR operations on the soft decision bits of the data

block in an attempt to correctly decode the data block." As Pukkila describes at paragraph 25, last sentence, block 205' is a "turbo equalizer." Block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and reinterleaving operations. Block 205' of FIG. 2 of Pukkila cannot be equated with an IR processing module. Further, blocks 305-318 do not disclose, suggest, or teach "performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block." Because Pukkila does not identically set forth this element of claim 1, Pukkila does not anticipate claim 1.

In conclusion, Pukkila fails to anticipate claim 1 for any and all of the reasons provided above. Further, because claims 3-5, 7, and 11 depend from claim 1, Pukkila fails to anticipate claims 3-5, 7, and 11 for at least these same reasons.

Claims 16 is not anticipated under 35 U.S.C. 102(b) by Pukkila

Independent claim 16 is directed to a "system for implementing Incremental Redundancy (IR) operations in a wireless receiver." This system includes:

a baseband processor that is operable to receive analog signals corresponding to a data block and to produce samples of the analog signals;

an equalizer that is operable to receive the samples from the baseband processor, to equalize the samples, and to produce soft decision bits of the data block;

a system processor that is operable to receive the soft decision bits of the data block;

a plurality of IR processing module registers communicatively coupled to the system processor;

an IR processing module communicatively coupled to the system processor and to the plurality of IR processing module registers;

wherein the system processor is operable to configure the plurality of IR processing module registers and to initiate operation of the IR processing module of the wireless receiver; and

wherein the IR processing module is operable to access the plurality of IR processing module registers, to receive the soft decision bits of the data block, and to perform IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block.

The Office Action equates block 203 of Pukkila (Ampl., A/D) with the baseband processor of claim 16. Block 203 of Pukkila is a combined amplifier and analog to digital converter. A combined amplifier and analog to digital converter is simply not equivalent to a baseband processor. A baseband processor, in addition to performing amplification and analog-to-digital conversion operations, is capable of performing significant other baseband processing operations, as is described in the specification of the present application. Thus, the combined amplifier and analog to digital converter of Pukkila block 203 does not identically set forth the baseband processor of claim 16. For this reason, Pukkila does not anticipate claim 16.

The Office Action equates four elements of claim 16 with block 205' of Pukkila. Firstly, the Office Action equates the equalizer of claim 16 with block 205 (of block 205') of FIG. 2 of Pukkila. Secondly, the Office Action equates the plurality of IR processing module registers with block 205' of FIG. 2 (and operations of FIG. 3) of Pukkila. Thirdly, the Office Action equates the system processor with block 205' of FIG. 2 (and operations of FIG. 3) of Pukkila. Fourthly, the Office Action equates the IR processing module with block 205' of FIG. 2 (and operations of FIG. 3) of Pukkila. Equating block 205' with multiple claim elements is impermissible in making an anticipation rejection. Each teaching of a prior art reference can only be used to meet one claim

element. Because block 205' is cited against multiple elements of claim 16, Pukkila does not anticipate claim 16.

Block 205' of FIG. 2 of Pukkila cannot be equated to the system processor, the plurality of IR processing module registers, or the IR processing module of claim 16. As Pukkila describes at paragraph 25, last sentence, block 205' is a "turbo equalizer." Block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and reinterleaving operations. Block 205' of FIG. 2 and the related operations of FIG. 3 of Pukkila do not identically set forth the "system processor that is operable to receive the soft decision bits and to initiate IR operations" of claim 16. Block 205' of FIG. 2 and the related operations of FIG. 3 of Pukkila do not identically set forth the "plurality of IR processing module registers communicatively coupled to the system processor" of claim 16. Block 205' of FIG. 2 and the related operations of FIG. 3 of Pukkila do not identically set forth the "IR processing module operably coupled to the system processor that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits" of claim 16. Thus, Pukkila does not disclose the system processor, the plurality of IR processing module registers, or the IR processing module of claim 16. For each of these reasons, Pukkila does not anticipate claim 16.

Pukkila further fails to describe the interaction among the elements of claim 16. Pukkila does not describe how "the system processor is operable to configure the plurality of IR processing module registers and to initiate operation of the IR processing module of the wireless receiver." Further, Pukkila does not described how "the IR processing module is operable to access the plurality of IR processing module registers, to receive the soft decision bits of the data block, and to perform IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block." For these additional reasons, Pukkila does not anticipate claim 16.

In conclusion, Pukkila fails to anticipate claim 16 for any and all of the reasons provided above. Further, because claims 18-20, 22, 26, and 29 depend from claim 16, Pukkila fails to anticipate claims 18-20, 22, 26, and 29 for at least these same reasons.

Claims 1-7, 9-11, 13-22, 24-26, and 28-31 are not anticipated under 35 U.S.C. 102(e) by Parolari

The Office Action rejects claims 1-7, 9-11, 13-22, 24-26, and 28-31 under 35 U.S.C. 102(e) as being anticipated by Parolari (US 2004/0081248 A1, published April 29, 2004). In response to this rejection, Applicants point out that Parolari is not prior art under 35 U.S.C. 102(e). As stated in 35 U.S.C. 102(e), a reference is prior art when:

> "the invention was described in — (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States **only if** the international application designated the United States and **was published** under Article 21(2) of such treaty in the English language."

Parolari is a publication of application Ser. No. 10/680,122, filed October 8, 2003, which is a continuation of PCT/EP02/03881, filed April 8, 2002. Parolari does not state that PCT/EP02/03881 "was published under Article 21(2) of such treaty in the English language" as is required by 35 U.S.C. 102(e). The effective date of Parolari is therefore October 8, 2003. The present application has an effective filing date of December 9, 2002, based upon a

priority claim to 60/431,940. This effective filing date of December 9, 2002 predates the October 8, 2003 filing date of Parolari. Thus, Parolari is not prior art under 35 U.S.C. 102(e) and therefore does not anticipate claims 1-3, 5, 8-16, 18, 21-27, 30-32 and 34 under such section.

Claims 8, 12, 23, and 27 are not unpatentable under 35 U.S.C. 103(a) over Parolari as applied to claims 1 and 16, and further in view of Ramesh.

Parolari is not prior art to the present application for the reasons stated above. Because Parolari is not prior art to the present application, the 35 U.S.C. 103(a) rejection of claims 8, 12, 23, and 27 is improper and should be withdrawn.

All claims are now allowable and a notice of allowance is courteously solicited. Please direct any questions or comments to the undersigned attorney at the address indicated.

Respectfully submitted,

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